CLAIMS:

1. A voltage translator circuit (31) for employing a control signal referenced to a first reference voltage (11) to switch a drive output referenced to a second reference voltage (14), comprising:

(a) a pair of pull down devices (34,35), each receiving a control signal as a respective one of a pair of complementary signals;

(b) a pair of pull up devices (36,37), each in series with a respective one of the pair of pull down devices (34,36), and each being driven by a respective positive feedback signal reflecting a state of conduction of the pull up device; and

(c) current blocking devices (38,39), in series with a respective one of the pair of pull up devices (36,37), at least one of which having a control input for selectively impeding a current flowing in series to a respective pull down device (34,35).

2. The voltage translator according to claim 1, wherein the second reference voltage (14) is greater than the first reference voltage (11).

3. The voltage translator according to claim 1, wherein the pull down devices (34,35) are each NMOS transistors and the pull up devices (36,37) are each PMOS transistors.

4. The voltage translator according to claim 1, wherein the current blocking devices (38,39) are each PMOS transistors.

5. The voltage translator according to claim 1, wherein the positive feedback signal for a respective pull up device (36,37) is the node voltage at a junction between the other pull up device (37,36) and the pull down device in series (35,34).

6. The voltage translator according to claim 1, further comprising an inverter (16,17) for generating the pair of complementary signals for the pair of pull down devices (34,35).

7. The voltage translator according to claim 1, wherein one of the pair of current blocking devices (39) has a static control input (B) limiting a current flow therethrough and the other of the pair of current blocking devices (38) has an active control input (A) for selectively modulating a flow therethrough in dependence thereon.

8. The voltage translator according to claim 1, wherein each of said pair of current blocking devices (38,39) has a control input signal referenced to said second voltage reference (14).

9. The voltage translator according to claim 1, further comprising a complementary device transmission gate (32), wherein a pair of complementary outputs from the respective nodes between respective ones of the pairs of pull up devices (36,37) and pull down devices (34,35) drive control inputs of the complementary device transmission gate (32).

10. The voltage translator according to claim 1, wherein the first reference voltage (11) is a logic circuit supply voltage and said second reference voltage (14) is the supply voltage for a liquid crystal device (42).

11. The voltage translator according to claim 1, further comprising:

an inverter (16,17) for forming a complementary signal from the control signal;

a complementary device transmission gate (32), wherein a pair of complementary outputs from the respective nodes between respective ones of the pairs of pull up devices (36,37) and pull down devices (34,35) drive control inputs of the complementary device transmission gate (32),

wherein said pair of pull down devices (34,35), a pair of pull up devices (36,37), a pair of current blocking devices ((38,39), inverter (16,17) and complementary device transmission gate (32) are each formed on a silicon integrated circuit; and

a liquid crystal display device (42) disposed on a surface of the silicon integrated circuit (40) and being modulated by said complementary device transmission gate (32).

12. A matrix display panel comprising a voltage translator circuit as claimed in claim 1.

13. A method of translating a voltage control signal referenced to a first voltage reference (11) to switch a drive output referenced to a second reference voltage (14), comprising the steps of:

(a) providing a circuit (31) having a pair of branches, each branch having:

(i) a pull down device (34,35), respective branches receiving complementary components of the voltage control signal;

(ii) a pull up device (36,37), in series with a respective pull down device (34,35), and each being driven by a positive feedback signal reflecting a state of conduction of the pull up device (36,37); and

(iii) a current blocking device (38,39), in series with the pull up device (36,37), having a control input for impeding a current flowing in series to a respective pull down device;

(b) selectively blocking a current flow through one of the branches by operating the control input of one of the current blocking devices (38,39) while permitting current flow through the other branch;

(c) while current flow is selectively blocked in one of the branches, switching a state of the voltage control signal; and

(d) after switching a state of the voltage control signal, selectively permitting current flow through both branches.

14. The method according to claim 13, wherein the second reference voltage (14) is greater than the first reference voltage (11).

15. The method according to claim 13, wherein the pull down devices (34,35) are each NMOS transistors and the pull up devices (36,37) are each PMOS transistors, the current blocking devices (38,39) are each PMOS transistors, and the positive feedback signal for a respective pull up device (36,37) is the node voltage at a junction between the other pull up device (37,36) and the pull down device (35,34) in series with it.

16. The method according to claim 13, further comprising the step of receiving an input signal and inverting the input signal to form the complementary components of the voltage control signal.

17. The method according to claim 13, further comprising the step of controlling one of the current blocking devices (38,39) to achieve a state of partial conduction.

18. The method according to claim 13, further comprising the step of driving a complementary device transmission gate (32) with a pair of complementary outputs from the respective nodes in each branch between the pull up device (36,37) and the pull down device (34,35).

19. The method according to claim 13, further comprising the step of modulating an optical state of a liquid crystal display device (42) based on the voltage control signal.

20. The method according to claim 13, further comprising the steps of:

receiving an input signal and inverting the input signal with an inverter (16,17) to form the complementary components of the voltage control signal;

providing a complementary device transmission gate (32), wherein a pair of complementary outputs from the nodes between a pull up device (36,37) and pull down device (34,35) of a respective branch drive control inputs of the complementary device transmission gate (32);

providing a liquid crystal display device (42) disposed on a surface of the silicon integrated circuit (40); and

modulating an optical state of the liquid crystal display device (42) with the complementary device transmission gate (32),

wherein the pull down devices (34,35), pull up devices (36,37), current blocking devices (38,39), inverter (16,17) and complementary device transmission gate (32) are each formed in a silicon integrated circuit.